REMARKS

Examiner Interview summary

In a telephonic conversation with the Examiner on July 21, 2004, with the below-signed attorney, Andrew C. Walseth, no agreement was reached regarding the pending claims. The Examiner's rejections of claims 34-41 under 35 U.S.C. §112, first paragraph and claims 20-24, 27-33, 38 and 39 under 35 U.S.C. §112, second paragraph were maintained by the Examiner. The Examiner's objections under 37 C.F.R. §1.83(a) were also discussed.

The Examiner is invited to contact Applicant's Representatives if there are any changes or questions regarding this Examiner Interview Summary or if prosecution of this application may be assisted thereby.

Claim Amendments

Claims 20, 22, 27, 28, 32, 34, 38 and 41 are amended herein.

Claim Rejections Under 35 U.S.C. § 112

Claims 34-41 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. The Examiner states the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Applicant traverses the rejection and believes that claims 34-41 are allowable for the following reasons.

The Examiner rejected claims 34-41 and specifically maintaining that claims 34, 38 and 41 recited variables that were not defined. As detailed in the Applicant's Response of June 1, 2004, the Applicant disagrees with the Examiner's assertion, maintaining that X and Y represent nominal values of data bits and data connections and that the claims are defined by the relationship of X and Y as detailed in the specific claim. However, to further the examination of the present Application, the Applicant has amended independent claims 34, 38 and 41, herein, to remove the reference to these variables. The Applicant therefore maintains that claims 34, 38

and 41, as amended, are described by the specification in a way to enable one skilled in the art to make or use the invention. As claims 35-37 and 39-40 depend from and further define claims 34 and 38, respectively, they are also considered enabled.

Applicant therefore respectfully requests that the rejection of the claims 34-41 under 35 U.S.C. § 112, first paragraph, be withdrawn in light of the above arguments and that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Rejections Under 35 U.S.C. § 112, second paragraph

Claims 28-33 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Applicant traverses this rejection and feels that claims 28-33 are allowable for the following reasons.

The Examiner rejected independent claim 28 as indefinite, stating that "the term 'X' is not defined in the claim, such as 'where x is a positive integer greater than 1.'" (Final Office Action mailed July 29, 2004, Page 3) As detailed in the Applicant's Response of June 1, 2004, the Applicant disagrees with the Examiner's assertion, maintaining that the term "X" of claim 28, a "method of testing a memory device having X selectable tests," refers to a number of possible tests that the memory device can perform. This number is inherently an integer value and thus is sufficiently defined to render the claim definite.

However, to further the examination process of the present Application, the Applicant has amended independent claim 28 herein to define X as suggested by the Examiner. The Applicant therefore maintains that the term "X" of claim 28 is thus sufficiently defined to render the claim definite. *See, e.g.*, MPEP § 2173 and § 2173.02. As claims 29-33 depend from and further define claim 28 they are also considered to be allowable.

The Applicant therefore respectfully requests that the rejection of claims 28-33 under 35 U.S.C. § 112, second paragraph to be withdrawn.

Claims 20-24, 27, 32, 33, 38 and 39 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Applicant traverses this rejection and feels that claims 28-33 are allowable for the following reasons.

The Examiner rejected claims 20, 22-23, 27, 32-33 and 38-39 as indefinite, stating that the phrase "prohibiting the test mode" contained in claims 20, 22-23, 27, 32-33 and 38-39 is unclear. The Examiner further stated that "[f]or purposes of examination, the examiner will assume that the circuit is prohibited from entering the test mode." (Final Office Action mailed July 29, 2004, Pages 3-5) Applicant acknowledges that the Examiner's assumption is correct and that "prohibiting the test mode" refers to preventing the memory device from entering the test mode of operation. As detailed in the Applicant's Response of June 1, 2004, the Applicant disagrees with the Examiner's assertion of indefiniteness, maintaining that the expression "prohibiting the test mode" presents no uncertainty or ambiguity with respect to the question of scope or clarity of the claim and is the claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art.

However, as above, to further the examination process of the present Application, the Applicant has amended claims 20, 22, 27, 32 and 38 herein to define "prohibiting the test mode" as suggested by the Examiner as "prohibiting the circuit from entering the test mode." The Applicant therefore maintains that claims 20, 22, 27, 32 and 38, as amended, are thus sufficiently defined to render the claims definite. As claims 21, 23-24, 33 and 39 depend from and further define claims 20, 22, 27, 32 and 38, respectively, they are also considered to be allowable.

The Applicant therefore respectfully requests that the rejection of claims 20, 22-23, 27, 32-33 and 38-39 under 35 U.S.C. § 112, second paragraph to be withdrawn.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 7, 13, 16, 22, 25, 27, 28 and 29 were rejected under 35 U.S.C. § 102. The Applicant is confused by the format of the rejection, but is assuming that the Examiner is affirming her rejections of the Office Action mailed March 30, 2004, and will respond as such.

In the Office Action mailed March 30, 2004, claims 1-5, 7-12 and 14-27 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Roohparvar (U.S. Patent 5,526,364), claims 1-3, 7-9, 16 and 17 were rejected under 35 U.S.C. § 102 (e) as being anticipated by Akaogi et al. (U.S. Patent 6,550,028), and claims 28 and 29 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Fang et al. (U.S. Patent 5,802,071).

In the present Final Office Action, mailed on July 29, 2004, claims 1 and 7 were rejected by the Examiner under §102 (Final Office Action mailed July 29, 2004, Page 6), but no subsection of §102 or reference was cited in the rejection. Claims 7, 13, 16, 22, 25 and 27 were also rejected by the Examiner under §102 (Final Office Action mailed July 29, 2004, Page 6), and no subsection of §102 or reference was cited in the rejection. The Applicant assumes that the Examiner was affirming the rejection of claims 1, 7, 13, 16, 22, 25 and 27 under 35 U.S.C. §102 (b) as being anticipated by Roohparvar (U.S. Patent 5,526,364) and will respond as such.

Applicant respectfully traverses this rejection and feels that claims 1, 7, 13, 16, 22, 25 and 27 are allowable for the following reasons.

In maintaining the rejection, the Examiner stated that Roohparvar cites "appropriate test mode codes are placed on the I/O lines." The Examiner also stated that "[a]s the prior arts do not limit which input or I/O is being used the prior art rejection is maintained." Applicant respectfully disagrees and maintains that Roohparvar does limit the input and I/O that are used. The Applicant notes that Roohparvar details in Figure 1 that the address pad 12 is separate from the I/O pads 17 and is used in combination with the write enable (~WE) 11 to initiate the test and load the test code into the test code latch of memory device. Further, Roohparvar does not teach or disclose the address input as coupled to the test mode code latch 20 and, as noted by the Examiner, an AND gate 15 coupled to the high voltage detectors 13 and 14 requires that the Address line and WE must both be at a high voltage at the same time to load the test code from

the I/O lines into the test mode code latch 20. As such, it would be impossible for the Address input of Roohparvar to be used to input the test code as it is not coupled to the test mode code latch 20 and, in addition, it is utilized to trigger the loading of the test code. The Applicant also submits that one skilled in the art would not interpret the I/O lines of a memory as including the address lines. The Applicant submits that the position of the Examiner that the I/O lines of a memory as including the address lines impermissibly changes the principal operation of memory devices in general and, in particular, the principal of operation of the memory device disclosed in Roohparvar, to support the Examiner's rejection.

The Applicant therefore maintains that Roohparvar discloses a memory device which receives a test code on the I/O (bi-directional data) lines to select the test mode and enters the test mode and loads the test code upon receiving a high voltage on the ~WE and an address input. *See, e.g.*, Roohparvar, Abstract, Figure 1, elements 11, 12, 17 and 20, column 2, line 54 to column 3, line 3, and column 3, lines 7-43.

Further, if the Examiner is relying on the inherent disclosure of the I/O lines of Roohparvar including address lines in rejecting the claims 1, 7, 13, 16, 22, 25 and 27 under 35 U.S.C. §102(b), or is taking official notice of Roohparvar disclosing a synchronous system the Examiner's rejection is also erroneous, as detailed below.

Inherent elements of a prior art reference may also be used in rejecting claims under 35 U.S.C. §102 or §103. To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. Once the examiner makes a prima facie case for an element being inherent, the burden shifts to the applicant to refute the case for inherency by reasoning or by providing extrinsic evidence. *See, e.g.*, MPEP §2112.

The Applicant notes that nowhere does Roohparvar specifically disclose that the I/O lines include address lines. If the Examiner maintains that the I/O lines include address lines is an inherent element of Roohparvar, or is taking office notice of this fact, the Applicant respectfully submits that the Examiner has the burden of providing supporting reasoning for this assertion. In

particular, the Applicant respectfully submits that the Examiner has the burden of proving that the inherent element must of necessity only work in the manner of the Applicant's disclosed invention. If any other interpretation is possible for the inherent element relied upon for the rejection, the rejection cannot be maintained. (*See,* MPEP §2112 and §2163.07(a)). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). (*See,* MPEP §2112).

Applicant respectfully submits that the allegedly inherent characteristic of the I/O lines including address lines does not necessarily flow from the teachings of the applied prior art of Roohparvar and would be so recognized by persons of ordinary skill. In other words, there is no support that loading a test code across I/O lines necessarily implies that the test code is inherently loaded across the address inputs, particularly, given that Roohparvar discloses that one of the test mode initiating inputs is an address input. Triggering the loading of a test code across I/O lines with an address line is not the same as loading the test code across the address inputs.

Applicant also submits that there are multiple possible interpretations for the fact that the memory device of Roohparvar loads the test code across the I/O lines, besides the conclusion that the memory device inherently discloses loading the test code across the address inputs. One possible alternative interpretation is that the I/O lines of the memory device of Roohparvar includes only the data lines, which are utilized to load the test code to the memory device and that a specific combination of high voltage on the address inputs and/or control lines are used to trigger this loading. This is consistent with the common understanding in the art that I/O lines are bi-directional while address lines are not.

Applicant also submits that if the Examiner maintains that Roohparvar inherently describes loading a test code across address lines, that such inherency may be rebutted by the Applicant by the submission of extrinsic evidence to the contrary. A *prima facie* case of inherency by the Patent Office may be rebutted by the Applicant by an appropriate showing. Therefore, the *prima facie* case can be rebutted by evidence showing that the prior art products do not necessarily possess the characteristics of the claimed product. *In re Best*, 562 F.2d at 1255, 195 USPQ at 433. (*See*, MPEP §2112.01). As stated above, the Applicant submits that

Roohparvar itself in Figure 1 discloses that the address inputs are not part of the I/O lines and thus rebuts the Examiner's position that they are inherently part of the I/O lines.

As such, because of the fact that a person of ordinary skill in the art would not recognize that I/O lines utilized for the test code input for the memory device of Roohparvar would necessarily include the address lines, and the fact that there are multiple possible interpretations to the I/O lines of Roohparvar used for inputting a test code to the memory device, the Examiner has not shown the necessity required for inherency in claiming Roohparvar describes a memory device utilizing address inputs to load test code data into the memory device. Therefore as Roohparvar does not inherently describe a memory device that loads a test code over the address inputs, the Applicant submits that Roohparvar fails the all element rule for Applicant's independent claims 1, 7, 13, 16, 22, 25 and 27.

Applicant therefore respectfully maintains that Roohparvar does not teach or disclose a memory device that initiates a test mode selected by test codes received on the address inputs. Applicant contends that address inputs do not correspond to Roohparvar's I/O lines.

Applicant's claim 1 recites, in part, "address input connections to receive externally provided signals" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the externally provided signals." As detailed above, Applicant submits that Roohparvar fails to teach or disclose such a non-volatile memory device that initiates a test mode selected by externally provided signals received on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 1.

Applicant's claim 7 recites, in part, "address input connections to receive externally provided address and test mode code signals" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the test mode code signals." As detailed above, Applicant submits that Roohparvar fails to teach or disclose such a flash memory device having such control circuitry that places the non-volatile memory in a test mode selected by test mode code signals received on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 7.

Applicant's claim 16 recites, in part, "selecting a test mode in response to a test code provided on address inputs." As detailed above, Applicant submits that Roohparvar fails to teach

or disclose such a method that selects a test mode in response to test codes received on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 16.

Applicant's claim 13 recites, in part, "address input connections to receive externally provided address and test mode code signals from the external memory controller" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the test mode code signals." As detailed above, Applicant submits that Roohparvar fails to teach or disclose placing a memory device in a test mode selected by test codes received on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 13.

In regards to claim 22, the Applicant notes that Applicant's claim 22 recites, in part, "selecting a test mode in response to a test code provided on the address inputs." As detailed above, Applicant submits that Roohparvar fails to teach or disclose selecting a test mode in response to a test code provided on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 22.

Applicant's claim 25 recites, in part, "receiving a test code command on address input connections" and " wherein the test code command instructs the memory device to perform a selected test operation." As detailed above, Applicant submits that Roohparvar fails to teach or disclose receiving a test code command on address input connections and wherein the test code command instructs the memory device to perform a selected test operation. As such, Roohparvar fails to teach or disclose all elements of independent claim 25.

Applicant's claim 27 recites, in part, "selecting a test mode in response to a test code provided on the address inputs." As detailed above, Applicant submits that Roohparvar fails to teach or disclose selecting a test mode in response to a test code provided on the address inputs. As such, Roohparvar fails to teach or disclose all elements of independent claim 27.

Applicant respectfully contends that claims 1, 7, 13, 16, 22, 25 and 27 have been shown to be patentably distinct from the cited reference. As claims 2-6, 8-12, 14-15, 17-21, 23-24 and 26 depend from and further define claims 1, 7, 13, 16, 22 and 25, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 1-27.

In the present Final Office Action, mailed on July 29, 2004, claims 7, 13, 16, 22, 25 and 27 were also rejected by the Examiner under §102 (Final Office Action mailed July 29, 2004, Page 6), and no subsection of §102 or reference was cited in the rejection. The Applicant assumes that the Examiner was, in addition to the above rejection of claims 7, 13, 16, 22, 25 and 27 over Roohparvar, affirming the rejection of claims 1, 7 and 16 under 35 U.S.C. §102(e) as being anticipated by Akaogi et al. (U.S. Patent 6,550,028) and will respond as such. Applicant respectfully traverses this rejection and reserves the right to swear behind the cited reference. The Applicant feels that claims 1, 7 and 16 are allowable for the following reasons.

Applicant continues to maintain, as also stated by the Examiner in the Final Office Action, mailed on July 29, 2004, that Akaogi et al. teaches a non-volatile memory which allows the threshold voltage distribution of its floating gate memory array to be tested. The non-volatile memory device of Akaogi et al. does this by entering a test mode upon receiving specified combination on the chip enable 202, output enable 204, write enable 206, accelerate input 208, and reset input 210. An analog test voltage can then be directly applied through the ready/busy input 212 to the floating gate transistors selected by the address applied to the address inputs 102 to test their threshold voltage levels. Results of the threshold voltage test (the transistors that have been programmed at the applied test voltage) are read from the data output 192 in 8 or 16 bit result modes, dependent on a BYTE input pin that selects byte or word output in normal or test mode of operation. *See, e.g.*, Akaogi et al., Figures 1 and 2, column 14, lines 31-62, and column 12, line 30 to column 13, line 50.

Applicant notes that Akaogi et al. has only one test mode entered upon receiving specified combination on the chip enable 202, output enable 204, write enable 206, accelerate input 208, and reset input 210 and that Akaogi et al. does not select the test mode based on the external signals applied to the address inputs. The Applicant further notes that the address inputs of Akaogi et al. input the address of the memory cell to be tested for threshold voltage, not test codes, and, as such, the address inputs cannot be used to select the test mode.

Applicant therefore respectfully maintains that Akaogi et al. does not teach or disclose a memory device that initiates a test mode selected by externally provided signals (test codes) received on the address inputs. Applicant contends that a memory device that selects test modes to execute from signals provided on the address inputs do not correspond to Akaogi et al.'s single voltage threshold test mode which is entered by the specified combination on the chip enable, output enable, write enable, accelerate input and reset input lines.

Applicant's claim 1 recites, in part, "address input connections to receive externally provided signals" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the externally provided signals." As detailed above, Applicant submits that Akaogi et al. fails to teach or disclose such a non-volatile memory device having control circuitry that initiates a test mode selected by externally provided signal received on the address inputs. As such, Akaogi et al. fails to teach or disclose all elements of independent claim 1.

Applicant's claim 7 recites, in part, "address input connections to receive externally provided address and test mode code signals" and "control circuitry coupled to the address input connections to place the non-volatile memory device in a test mode selected by the test mode code signals." As detailed above, Applicant submits that Akaogi et al. fails to teach or disclose such a flash memory device that initiates a test mode selected by test codes received on the address inputs. As such, Akaogi et al. fails to teach or disclose all elements of independent claim 7.

Applicant's claim 16 recites, in part, "selecting a test mode in response to a test code provided on address inputs." As detailed above, Applicant submits that Akaogi et al. fails to teach or disclose such a method that initiates a test mode selected by test codes received on the address inputs. As such, Akaogi et al. fails to teach or disclose all elements of independent claim 16.

Applicant respectfully contends that claims 1, 7 and 16 have been shown to be patentably distinct from the cited reference. As claims 2-6, 8-12 and 17-21 depend from and further define claims 1, 7 and 16, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(e) and allowance of claims 1-12 and 16-21.

In the present Final Office Action, mailed on July 29, 2004, claims 28 and 29 were also rejected by the Examiner under §102 (Final Office Action mailed July 29, 2004, Page 8), and no subsection of §102 or reference was cited in the rejection. The Applicant assumes that the Examiner was, in addition to the above rejection of claims 7, 13, 16, 22, 25 and 27 over Roohparvar and Akaogi et al., affirming the rejection of claims 28 and 29 under 35 U.S.C. §102(b) as being anticipated by Fang et al. (U.S. Patent 5,802,071) and will respond as such. Applicant respectfully traverses this rejection and feels that claims 28 and 29 are allowable for the following reasons.

Applicant continues to maintain that Fang et al. teaches a micro-controller and test machine that can execute a test of the micro-controller from an external test circuit, a built-in test circuit, and an test application to provide a flexible test pattern. *See, e.g.*, Fang et al., Abstract, Figures 3 and 4, column 2, line 60 to column 3, line 58.

The Examiner states that Fang et al. discloses "[t]he ROM read-out device 40 is used for reading the program code from the application memory 34 to test whether the application program memory 34 can be read properly, so that the application program stored therein can be executed properly." (Fang et al. column 3, lines 21-26) and therefore Fang et al. does teach testing of memory. The Applicant disagrees with this assertion and notes the name of the "ROM read-out device 40" and that the Abstract of Fang et al. states that "(g) a ROM read-out device electrically connected to the multiplexer and the application program memory for reading program codes from the application program memory to facilitate the test instrument to make a comparison." (Fang et al., Abstract) The Applicant therefore asserts that Fang et al. does not disclose testing the memory, but merely reading the program codes out of the memory of the microcontroller to verify the stored data content.

Furthermore, in addition to whether Fang et al. discloses a method of testing memory devices, the Applicant has carefully reviewed Fang et al. and has found no mention of address lines or the use of address lines to input test code to select one of X selectable tests.

Applicant therefore respectfully maintains that Fang et al. does not teach or disclose a method of testing a memory device, but a method of testing a micro-controller. The Applicant

further maintains that Fang et al. does not teach or disclose a memory device that initiates a test mode selected by test codes received on the address inputs, but a micro-controller that selects test modes and reads test executables through separate data "channels". Applicant contends that memory device address input connections do not correspond to Fang et al.'s channels.

Applicant's claim 28 states, in part, "a method of testing a memory device", and "selecting one of the X selectable tests using a test code provided on address input connections." As detailed above, Applicant submits that Fang et al. fails to teach or disclose such a method of initiating a test mode selected by test codes received on the address inputs. As such, Fang et al. fails to teach or disclose all elements of independent claim 28.

Applicant respectfully contends that claim 28 has been shown to be patentably distinct from the cited reference. As claim 29 depends from and further defines claim 28 it is also considered to be in condition for allowance. Accordingly, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 28 and 29.

Rejections Under 35 U.S.C. § 103

In the Office Action mailed March 30, 2004, the Examiner also rejected claims 4-6, 10-12, 13-15 and 18-19 under 35 U.S.C. §103 (a) as being unpatentable over Akaogi et al. (U.S. Patent 6,550,028) in view of Sher et al. (U.S. Patent 6,154,851). In the present Final Office Action, mailed July 29, 2004, the Examiner did not affirm her rejection of claims 4-6, 10-12, 13-15 and 18-19 under 35 U.S.C. §103 (a). The Applicant therefore assumes that the rejection of these claims is withdrawn.

If the Examiner is maintaining her rejections of claims 4-6, 10-12, 13-15 and 18-19 under 35 U.S.C. §103 (a), the Applicant, as stated in the Response of June 1, 2004, respectfully traverses this rejection and feels that claims 4-6, 10-12, 13-15 and 18-19 are allowable for the following reasons.

Applicant contends that it has shown claims 1, 7 and 16 to be patentably distinct from the Akaogi et al. reference. The secondary reference of Sher et al. fails to overcome the deficiencies of the Akaogi et al. reference. Thus, claims 1, 7 and 16 are patentably distinct from the cited references, either alone or in combination. As claims 4-6, 10-12 and 18-19 depend from and further define one of claims 1, 7 or 16, these claims are also believed to be allowable.

In regards to independent claim 13, the Applicant respectfully submits that, as stated above, Akaogi et al. fails to teach or disclose a memory device that initiates a test mode selected by external signals (test codes) received on the address inputs. As such, Akaogi et al. fails to teach or suggest all elements of independent claim 13. In addition, Sher et al. also does not teach or disclose a memory device that initiates a test mode selected by test codes received on the address inputs. Therefore combining the elements of Akaogi et al. with Sher et al. does not teach or suggest all elements of claim 13. The Applicant therefore maintains that claim 13 is thus allowable over Akaogi et al. and Sher et al., either alone or in combination. As claims 14-15 depend from and further define claim 13, claims 14-15 are also deemed allowable.

Applicant respectfully contends that claims 4-6, 10-12, 13-15 and 18-19 as pending have been shown to be patentably distinct from the cited references, either alone or in combination. Accordingly, Applicant respectfully requests reconsideration and allowance of claims 4-6, 10-12, 13-15 and 18-19.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 9/8/04

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